FIBER CHANNEL WORKSTATIONS INTERCONNECTION THROUGH ATM LOCAL NETWORK: INTERWORKING ISSUES

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RESUMO

O Fibre Channel Standard (FCS) é um padrão emergente que possibilita um transporte eficiente para protocolos de comunicação já existentes, tais como Intelligent Peripheral Interface (IPI), Small Computer System Interface (SCSI) e High Performance Parallel Interface (HIPPI).
Este trabalho endereça os problemas de interconexão entre workstations com interfaces FCS e Comutador Asynchronous Transfer Mode (ATM). Em particular apresenta-se o projeto de uma FCS/ATM InterWorking Unit (IWU) com alto desempenho (vazão). Um protocolo especializado para a segmentação e reassemblamento, denominado FCS/ATM Protocol (FAP), foi definido para garantir a transparência dos protocolos FCS.
As características do hardware e do software da IWU são descritas e seu desempenho é avaliado através da simulação.
A avaliação do desempenho mostra que valores de vazão próximos à largura de faixa do enlace ATM podem ser obtidos dependendo da disciplina utilizada no gerenciamento dos buffers da IWU.

ABSTRACT

The Fiber Channel Standard (FCS) is an emerging standard for providing a common efficient transport vehicle for existing channel protocols like Intelligent Peripheral Interface (IPI), Small Computer System Interface (SCSI), and High Performance Parallel Interface (HIPPI). This paper deals with the interconnection issue of FCS-based workstations through an ATM switch. In particular, the design of a high throughput FCS/ATM InterWorking Unit (IWU) is presented. A specialized segmenting and reassembly protocol, named FAP, has been defined in order to guarantee the transparency of the end-to-end FCS protocols. The hardware and software characteristics of the IWU are described and its performace evaluated by a simulation study. Performance evaluation results show that throughput values approaching available ATM link band width can be achieved depending on the discipline utilized to manage the IWU buffers.

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1. INTRODUCTION

In local area very high speeds are desired to support a set of emerging sophisticaated applications like video distribution, computer imaging, multiprocessing in super and parallel computers, distributed file access and so on.
The Fiber Channel Standard (FCS) [1] addresses very high throughput issues in geographical limited networks. It provides a common efficient transport vehicle for existing upper layer protocols like Intelligent Peripheral Interface (IPI), Small Computer System Interface (SCSI) and High Perfofmance Parallel Interface (HIPPI). FCS is optimized for transfer of large blocks of data such as used for file transfer between processors (supercomputers, mainframes), high speed storage peripherals (disks and tapes), communications, visualization devices (frame buffers) and real time data acquisition units.
Contextually, ATM technology is gaining a wider and wider acceptance to provide a switching platform to interconnect high speed workstations and local shared medium network structures (Ethernet, FDDI etc.)
This paper is focused on the interconnection of FCS based workstations through an ATM switching fabric. In particular, the design of a FCS/ATM InterWorking Unit (IWU) is described allowing interconnection of an FCS link at 265.625 Mbit/s with an ATM link at 155.520 Mbit/s. This project has been developed in the framework of the Telecommunication Project supported by the Italian National Research Council (CNR) [2] [3].

The main goals of the IWU design are:

- to allow a completely transparent support of FCS procedures;
- to achieve the best throughput performance by allowing the full exploitation of the ATM link bandwidth.

Experiences in protocol interworking exposed a significant performance degradation if the protocol relaying functions are not optimized and if functions are not performed fast enough creating bottlenecks in the interworking unit. Therefore, in order to achieve maximum throughput performance, some specific arrangements have been adopted:

i) definition of an ad-hoc AAL protocol, called FCS/ATM Protocol (FAP), in order to avoid useless replications of functions and to allow transfer of FCS dedicated control information;

ii) hardware implementation of FAP functionalities and, in general, of all functions concerning data transfer phase;

iii) software handling of signalling phases (login, connection establishment, disconnection etc.).

A further key element to achieve optimum throughput performance consists in a careful design of system parameters to support flow control procedures of FCS

protocol. This feature has to be considered due to the difference between the bit rates sustained by FCS and ATM links. Two basic elements have to be taken into account:

i) a proper dimensioning of segmenting buffer at IWU;

ii) a proper tuning of negotiation procedure of the window size perfomed during the login phase. Moreover, the impact of the delay caused by the ATM node has to be taken into account. These aspects have been analyzed by simulation (they are not addressed in this paper). Performance evaluation results show that obtainable througput stricly depends on the handling discipline utilized in the IWU buffer.

This paper is structured in 5 sections. The basic FCS features having impact on the IWU funcionalities are summarized in Sec. 2. Section 3 is focused on the description of IWU functionalities in terms of protocol stack; the FAP protocol is also presented and hardware and software architectures are described. Finally, Sec. 4 presents software performance, whereas results of IWU performance evaluation are discussed in Sec. 5.

2. The Fibre Channel Standard

The FCS is logically a bidirectional point-to-point serial data channel structured for high performance capability. Physically, FCS can be an interconnection of multiple communications port, called N-port, interconnected through a switching network, called Fabric. In our context, a hub switch of an ATM LAN implements the fabric concept. A fabric access port, connected to an N-Port, is called F-Port. Figure 2.1 shows the point-to-point and fabric topology foreseen by FCS.

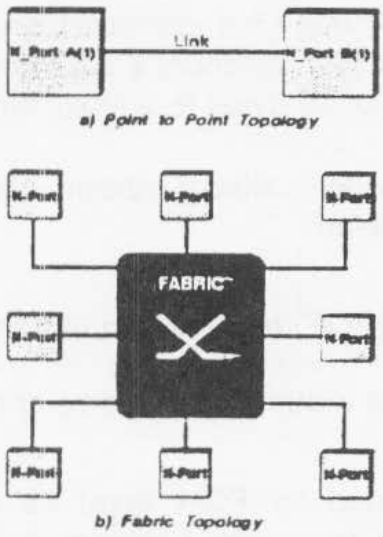

Figure 2.1 - Topologies

In Figure 2.2, the FCS protocol stack is shown. FC-3 and FC-4 layers constitute the interface to upper layer protocols. In particular, FC-3 provides a set of services

which are common across multiple ports of an FCS node. FC-4 maps upper layer protocols to FCS functionalities. FC-0, FC-1 and FC-2 are responsible for communication tasks and constitute the Fibre Channel Physical and Signalling Interface (FC-PH).

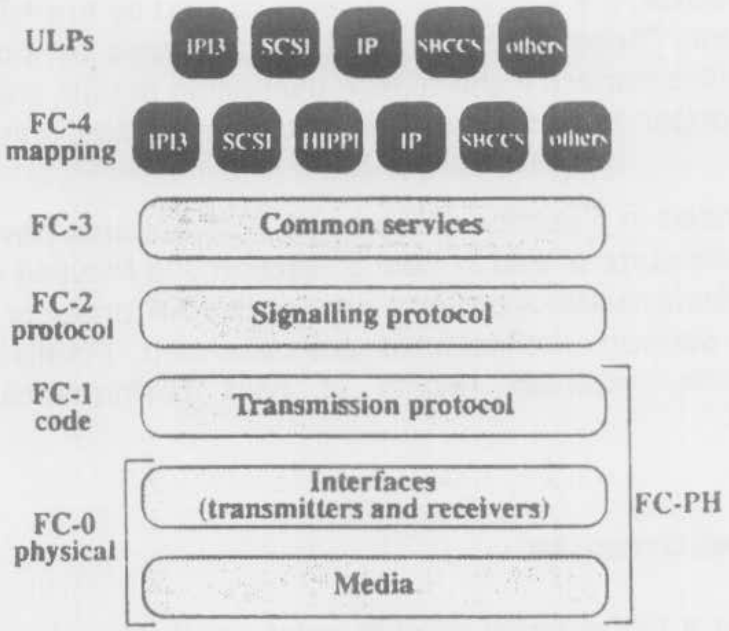

Figure 2.2 - Protocol stack for FCS

FC-0 defines the physical link characteristics. FCS enables speeds of 265 Mbit/s, 531 Mbit/s or 1.06 Gbit/s. Twisted pairs, coaxial calbes or optical fibers can be used depending upon distance to be bridged. A 8b/10b line doce (the same as that used in the 155 Mbit/s ATM forum Private LAN interface) is used for synchronization and for conveying additional control and commands information. FCS frame has variable length ranging from a minimum of 36 bytes to a maximum of 2148 bytes.

Some particular data sequences, called Ordered Sets, are used for signalling purposes. The sequences are used:

i) to indicate the start of frame (SOF) and the end of frame (EOF);

ii) to indicate specific conditions within a port (active or recovery states).

The ordered sets are generated by FC-1 level as well as 8b/10b coding and decoding. Ordered Sets always begin with a special character named K28.5.
FC-2 level serves as the transport mechanisms of FCS. It is basically a data link protocol and performs functions related to establishment, release and control of connections. FC-2 is structured in three classes of service: Class 1 that only supports point-to-point dedicated connections. Unacknowledged and acknowledged services are provided by Class 2 and 3, respectively.

In order to eliminate possible redundancies that could degrade resulting IWU throughput performance, functions performed by FC-PH having an impact on IWU functionalities need to be identified. These functions are:

i) detection of frame bit errors; it uses a CRC-32, in addition, a code violation, exploiting 8b/10b encoding, could be also used;

ii) detection of missing frames; frame loss is detected by using the Relative offset which is specified in the parameter field of the frame header; the Relative Offset is a FC-2 parameter indicating the displacement of the first data byte of each frame payload with reference to the base address, specified by the upper layer protocols at the sending end, for a block of data; using this information, dropped frames could be detected when a gap is detected in the offset field;

iii) frame delineation; it is performed using the encoded sequences SOF and EOF, 14 different sequences are used;

iv) flow control, two types of flow control are implemented: 1) end-to-end flow control (used between N-ports) that is managed by means of a window mechanism; the window size is negotiated during the connection set-up (N-Port Log-in phase); 2) buffer-to-buffer flow control (used between N-port and F-port) that is managed by means of Receive Ready (R-RDY) primitive signals.

3. IWU Architecture

Figure 3.1 shows the project scenario; the source and destination N-Ports represent user workstations with FCS interfaces. The local and remote F-Ports represent IWUs. The two IWUs are connected through a local ATM switch. In the following we describe the IWU functionalities by referring to a single IWU, namely the Local IWU. The IWU only implements bridging functions and supports Class 1 service of FC-2 layer of FCS.

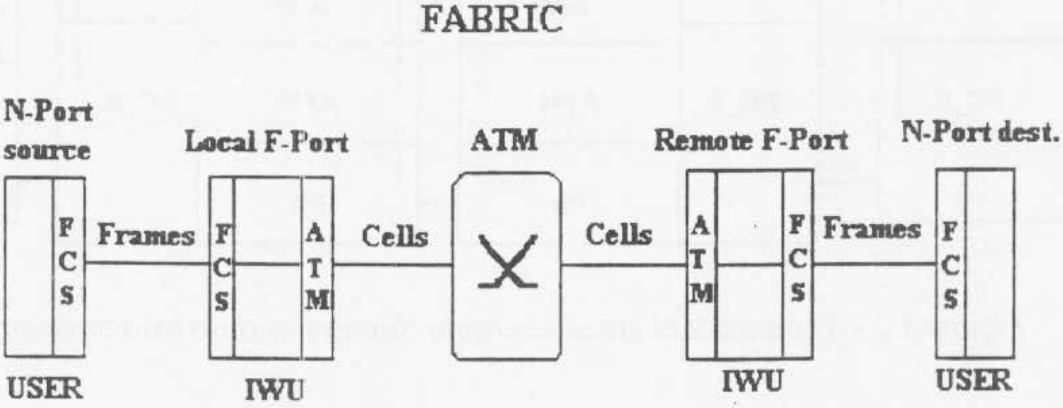

Figure 3.1 - "Fabric Model" and Project Scenario

3.1 - FCS/ATM PROTOCOL

The definition of the interoperability level between FCS and ATM basically means to define those functions that have to be carried out within the Adaptation Layer (AAL) for obtaining an efficient delivery of cell streams over a connection between two N-ports.
It is well known that AAL is divided in two sublayers: Segmentation and Reassembly (SAR) and Convergence (CS). SAR sublayer performs, at transmitting side, the segmentation of protocol data unit coming from CS sublayer into a suitable size for the information field to ATM cells and, at receiving size, the reassembly of the original CS-PDU. The CS is service dependent and provides the AAL service at the AAL Service Access Point (SAP).
Considering FC-PH functions listed in the previous section, in order to reduce IWU processing overhead, it was decided to leave empty the CS sublayer and to implement only the SAR protocoal, named FCS/ATM Protocol (FAP). So, the CS-PDU handled by SAR is FCS frame sent by the end-systems. This choice can be justified by considering that FC-2 has all the means to recovery possible error conditions introduced by the ATM layer (i.e. cell loss, bit errors etc.)
Figure 3.2 depicts the IWU protocol stack during the data transmission phase .

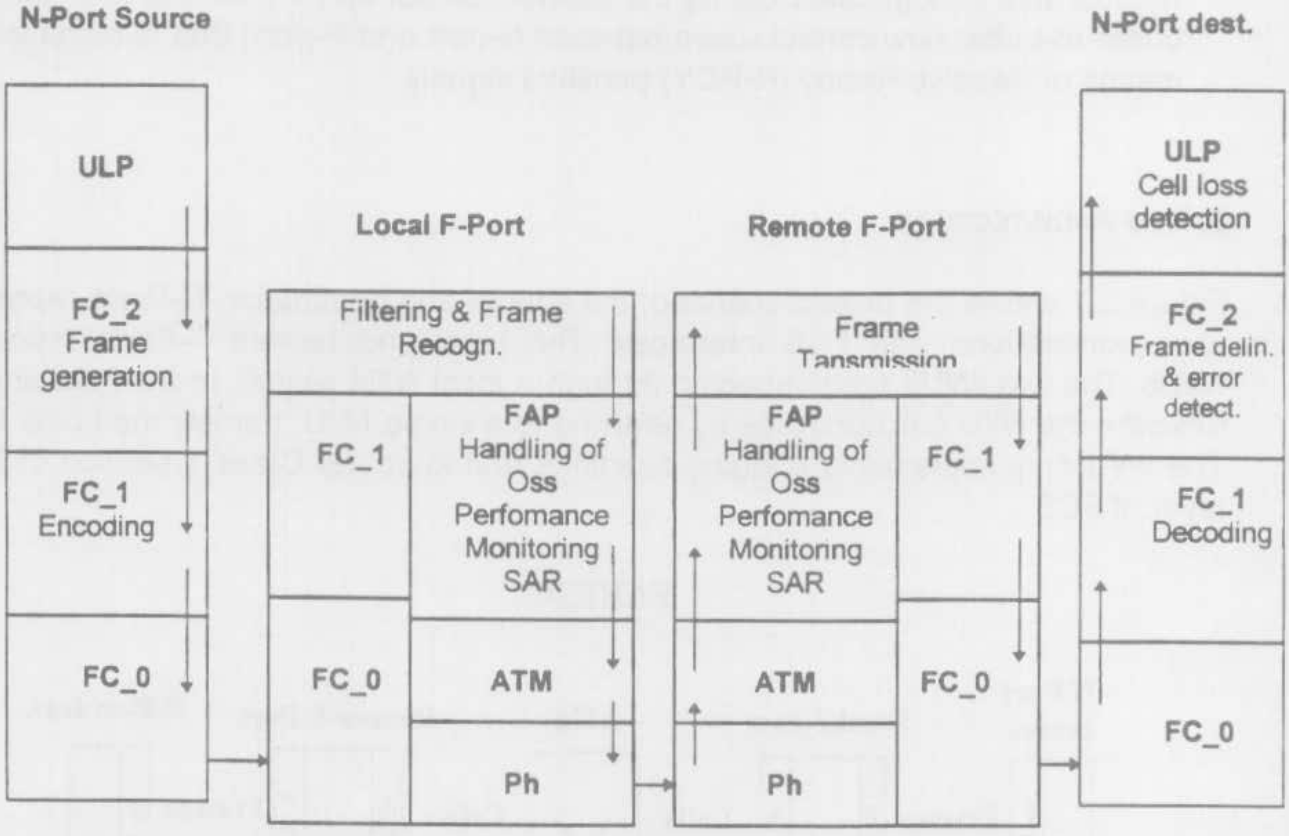

Figure 3.2 - The protocol stack scenario during the data transmission phase

FAP protocol functions are:

a) segmenting and reassembly;

a) mapping of specific Ordered Sets (Oss) (delimiters, primitive signals and sequences) in ATM cells;
b) monitoring of IWU performance.

FAP functions are performed via the combination of the bit PT2, i.e. the lowest order bit of the Payload Type (PT) field of the ATM cell header [4], and two bytes of the cell payload. So, the actual cell payloads is reduced to 46 bytes, and the additional overhead is limited to 4%. Figure 3.3 depicts the FAP bits within the ATM cell format.

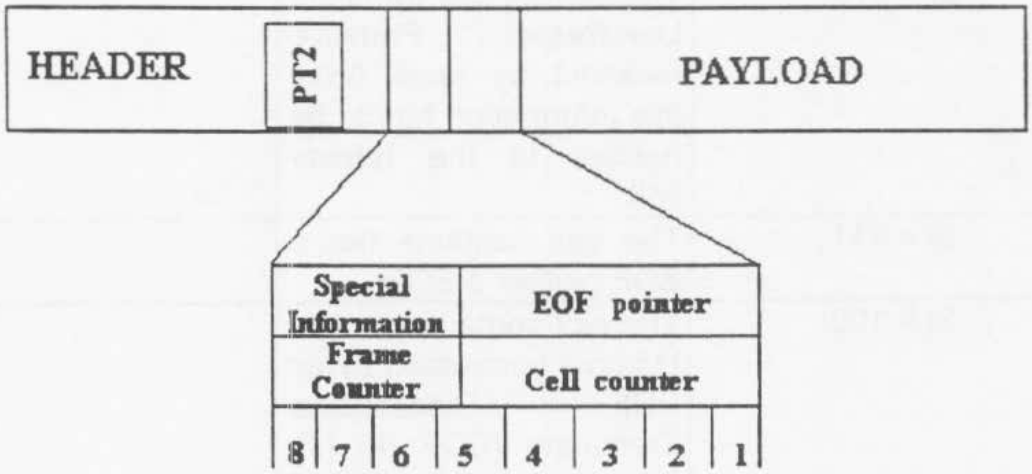

Figure 3.3 - The first two bytes of cell payload used to implement the FAP protocol.

According to [4], PT2 bit is available to transmit user-to-user information, FAP uses this bit to code SOF and EOF information: if PT2=0, the current cell is not the last cells of a FCS frame; otherwise (PT2=1), it carries an EOF.
The particular cell type is furtherly specified by using the Special Information (SI) field. This field is composed of three bits, its meaning depends on the value of PT2 bit; possible configurations are in Table 3.1.

Table 3.1 - Cell Types

	PT = 0	PT = 1
SI = 000	SOF cell and the cell payload contains a part of a FCS frame carried by multiple cells	This is a EOF cell and all the four characters of EOF ordered sets are contained in the current cell
SI = 001	SOF cell and the cell payload contains a whole FCS frame	This is an EOF cell but the four characteres of EOF ordered sets are divided in two cells
SI = 010	The current cell transfers Link-Reset Primitive received by local IWU; this information has to be notified to the remote IWU	
SI = 011	The cell contains nor a SOF neither a EOF	
SI = 100	The cell contains an Alk-H frame terminated by an EOF Disconnecte Terminate (EOF dt) [1]; this is a Link Control Frame which requires a buffer to buffer flow control; the port originating ACK-N/EOFdt requires a R-RDY response; figure 3.5 shows an example of buffer-to-buffer flow control	
SI = 101	The cell contains a SOFC	
SI = 110	The cell contains a PRJT.	

The EOF pointer field is composed of 5 bits, it codes, if needed, the offset (in bytes) of the first character of the EOF (K.28.5) inside the cell payload. Five bits are sufficient since cell payload is filled up on a word basis, a word being composed of a couple of bytes.

The Frame Counter field is composed of 2 bits, it contains the frame counter (mod. 4). Analogously, the Cell Counter filed (6 bits) counts (mod. 64) the cells belonging to the same FCS frame.

These two counters allow frame and cell loss to be detected.

Figures 3.4 and 3.5 show examples of frame exchange during Data transfer and N-Port login phase, respectively.

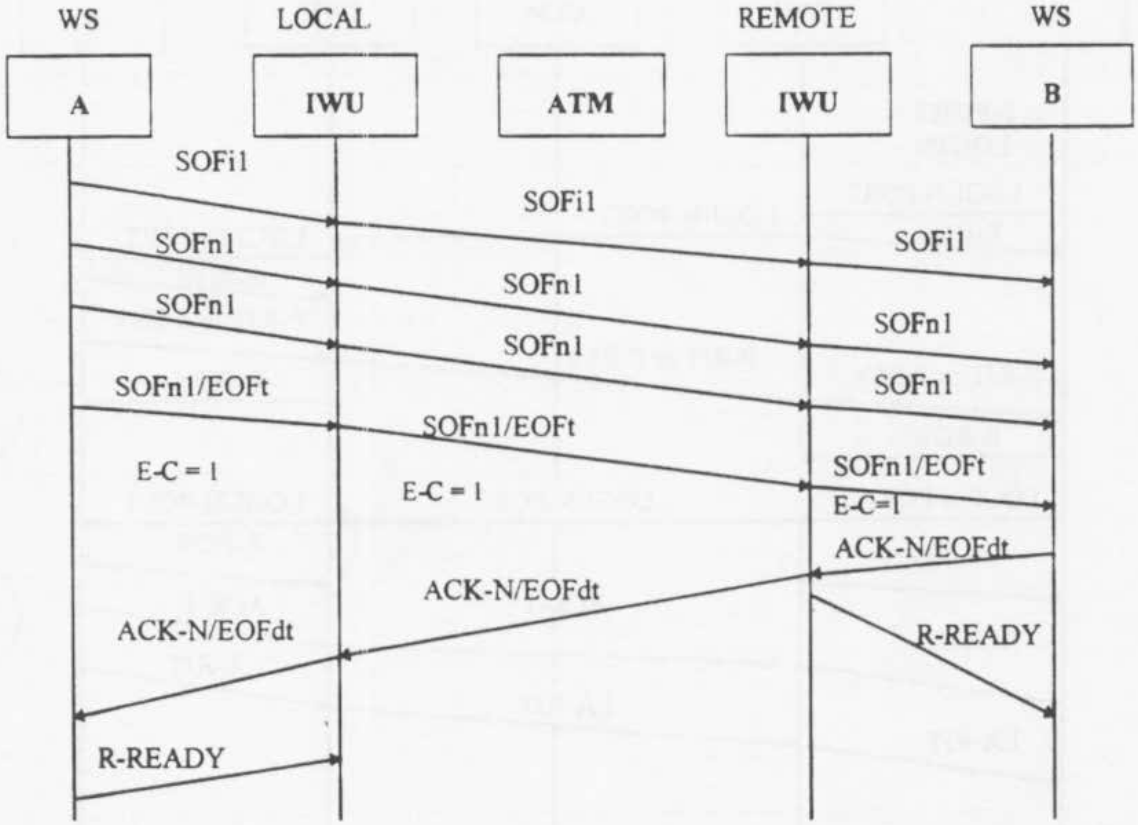

Figure 3.4 - Frame exchange during Data Transfer

In Figure 3.4 the WorkStation A emits FCS frames which are segmented by IWU and transferred to the remote IWU. The first FCS frame carries SOFi1 delimiter, indicating the beginning of Class 1 Service. Sucessive frames carries SOFn1 delimiters meaning normal frame transfer. Finally last frame carries both SOFn1 and EOFt delimiters. That means that a disconnect request has to be transferred and an acknowledgment is required. The ACK frame emitted by WS B will carry EOFdt delimiter indicating the acceptance of the disconnect request. When an ACK/EOFdt frame is received, a local R-READY signal has to be emitted by IWU.
Figure 3.5 shows three possible cases relevant to the N-port login phase: A and B are unsuccessful cases, whereas in the case C the login procedure is successfully completed. IWU properly maps control frames into ATM cells and generates R-RDY primitive signals according to buffer-to-buffer flow control procedures.

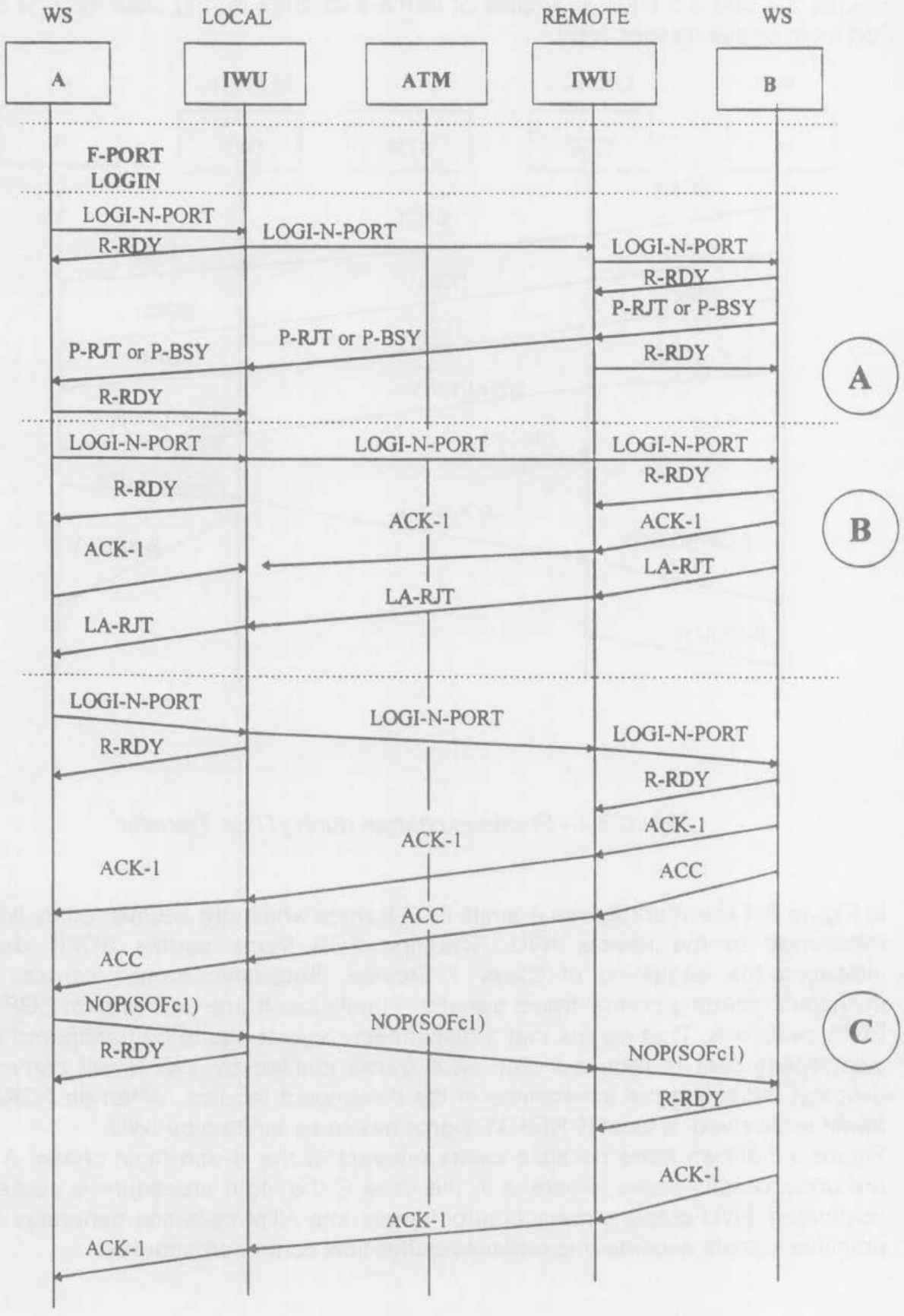

Figure 3.5 - Frame exchange during N-Port login

3.2 - HW ARCHITECTURE AND FUNCTIONALITIES

3.2.1 - FAP IMPLEMENTATION

The required IWU functions to implement the FAP were distributed in 4 boards (units) in order to solve thermal problemas inside the rack VME.
A functional block diagram of the IWU is shown in Figure 3.6. The IWU is divided into four funcional units: FCS-1 (that has the task to implement FILTERING), SAR-1 (that contains the circuits implementing SEGMENTATION), SAR-2 (which contains the REASSEMBLER) and FCS-2 (that has the task to accomplish the FCS interface and also contains the SENDER).
Each functional unit is implemented in a single board. These boards are interconnected via a VMEbus and were implemented using Logic Cell Array (LCA).
An additional board contains the Control Unit (CU). This board, (CPU 3 CE) is produced by FORCE Computers and is a VMEbus-based RISC SPARC unit completely compatible with the SUN SPARCstation 2.

The Operating System is the VxWorks, a high performance real-time OS which also supplies a powerful development environment for real-time applications.

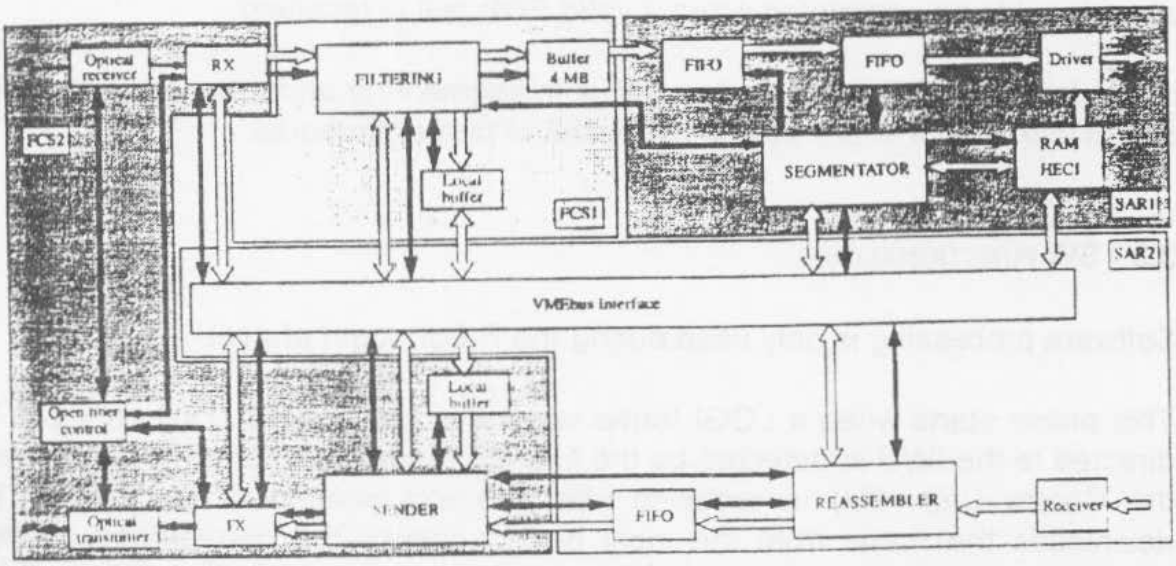

Figure 3.6 - Functional Block Diagram

The FCS2 contains the optical interface at 266 Mb/s and an Open Fiber Control unit (AMCC S2034 chip).
Receiving (RX) and trasmitting (TX) blocks are implemented by means of the AMCC transceiver chip-set (S2030 and S2031). They implement the FC0 and FC1 protocol functions.
The SENDER accepts FCS frames either from the SAR-2 unit (i.e. from de REASSEMBLER) or from the Local Buffer. It generates the proper signals to allow the FCS TX (AMCC S2030) to send the FCS link primitives to the N-Port.

FILTERING block receives frames in form of 16 bit words. It recognizes the frames addressed to either the IWU or the destination N-Port. In case the frame is addressed to the IWU, the frame is written into the Local Buffer and is available to be processed by the Control Unit. If the received frame must be forwarded it is written into a 4 Mbyte buffer and then processed for segmentation into ATM cells according to FAP rules. The Filtering also, implements a Finite State Machine (FSM) that will control what Primitive Sequences the IWU will send considering the previous Primitive Sequence transmitted and the validation of the received sequence. The validation is performed comparing the received Primitive Sequence with the expected one (the expected Primitive Sequence is defined by the Link Recovery Protocol).

The SAR-1 generates all the cell types described in sec. 3.1, by using control signals coming from the FILTERING block.

The Driver block drives the parallel ATM interface.

In SAR-2, tha ATM cells are received by the Receiver block. The REASSEMBLER restores the FCS frames starting from the SOF cell. Cells passing trough the REASSEMBLER are counted to verify that no cell has been lost. Frame is considered to be completed when a valid EOF cell is received.

It is to be noted that possible deadlocks in segmenting and reassembling processes, due to lack of EOFs, are solved by means of proper timeouts.

3.3 - SW FUNCTIONALITIES

Software processing is only used during the F-Port login phase.

This phase starts when a LOGI frame is received by the IWU. When a LOGI frame directed to the IWU is detected by the filtering block, an interrupt signal is issued to the Contro Unit (CU) in order to start the examination of the frame. The CU downloads the frame from the local buffer, checks the correctness of the CRC, prepares the ACK-1 answer frame and transfers it to the local buffer for transmission. After that, the analysis of the different fields of the received frame is performed. If all the requests contained in the LOGI frame are compliant with the IWU characteristics, an ACC frame is placed in the local buffer to be sent to the originating N-Port. The emission od the ACC frame ends the login phase.

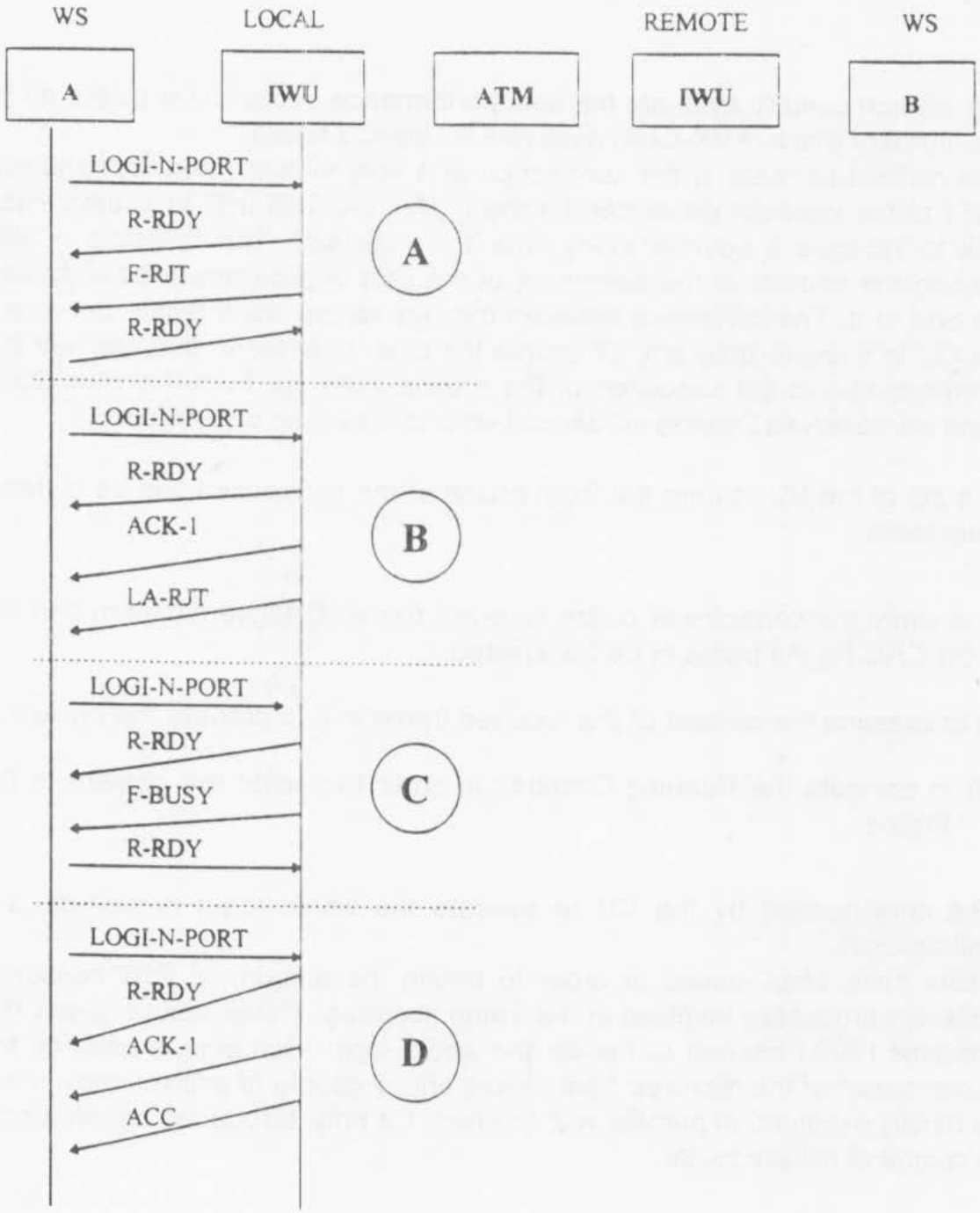

Figure 3.7 - F-Port login

Figure 3.7 summarizes all the possible cases that can happen during the F-Port login phase. The cases A, B and C occur when the F-Port login is not accepted. The successful case is shown in case D.

4. SOFTWARE PERFORMANCE

The software performance concern the time needed by the CU to handle all the frames exchanged during the login phase or the time needed to reject the connection in case the requests contained in the LOGI frame can not be satisfied.
This information is needed to properly size the FCS protocol timeouts.

The method used to evaluate the time performance of the CU is based on the use of the Auxiliary Block (AUX-CLK) available on the CU board.
This method consists in the connection of a very simple Interrupt handling Routine (IHR) to the interrupt generated by the AUX-CLK. The IHR in subject has only the task to increase a counter every time it is executed. The measure is obtained by reading the counter at the beginning of the part of program to be evaluated and at the end of it. The difference between the two values will indicate the time spent by the CU to execute program. Of course the time obtained in this way will include the overhead due to the execution of the routine itself but from the tests that we have done we observed that the introduced error is less than one percent.

The job of the CU, during the login phase of the connection can be divided in three main tasks:

i) to verify the correctness of the received frame (CRC verification) and to compute the CRC for the frame to be transmitted;

ii) to examine the content of the received frame and to prepare the answer rames;

iii) to compute the Running Disparity in order to decide the content of the End Of Frame.

The time needed by the CU to execute the whole login procedure is about 40 milliseconds.
Tests have been issued in order to obtain the amount of time consumed by the different processes involved in the frame handling. These tests showed that most of the time (90%) needed to handle the whole login exchange is used by task 1. The examination of the received frame takes only a couple of milliseconds . As the task 3 is mostly executed in parallel with the task 1 it only introduces an additional delay of a couple of milleseconds.

5. HARDWARE PERFORMANCE IN THE TRANSMISSION PHASE

In this section a simulation model is presented. This model has been developed in order to obtain the performance evaluation of the proposed IWU archtecture, focusing the actual implementation that allows the transmission of 4Mbyte data blocks with ACK-N flow control, in order to establish the proper values of protocol parameters.

5.1 - MODEL DESCRIPTION

The FCS/ATM interworking simulation model is shown in fig. 5.1.

The FCS source can assume two states, ON and OFF. The duration of each state follows a truncated exponential distribution. In the ON state, according to [1], the source generates valid FCS frames with the minimal interval time, equal to 6 idles.

The transmit buffer is reponsible of the flow control management; the frame transmission takes place according to the Class 1 service [1] utilizing the end-to-end flow control rules.

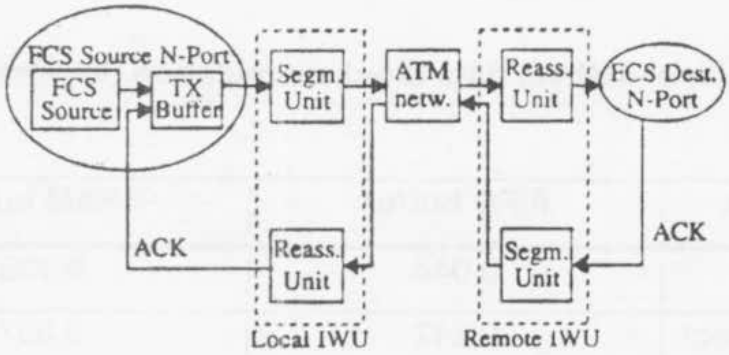

Figure 5.1 - FCS/ATM Interworking Scenario

The segmentation and reassembling unit are modeled as finite state machines, implementing the main features (filtering, segmentation buffers, RX and TX functions) of the IWU. They perform the segmentation of FCS frames into ATM cells at the transmitting side, according to the FAP protocol, and the FCS frame reassembly at the receiving side.
As for the actual implementation of the segmentation buffer, two possible solutions are considered: the first is based on a FIFO discipline (implemented by a Dual Port RAM); the second one is based on a Store and Forward discipline (implemented by a Static RAM); in the first case the segmentation process is carried out on the fly; in the second case a block of N frames must be received before initiating the segmentation process.

The ATM network has been modeled by means of a single ATM switch.

Due to the difference between the FCS and ATM bit rates, the ATM path is a bottleneck for the data transfer, so the IWU resources (i.e the segmentation buffer) and the FCS flow control parameters (i.e. window size, timeouts) must be dimensioned so as to maximize the throughput over the ATM path by guaranteeing no frame loss.

The role of the FCS dest. N-Port is generate an ACK message according to the flow control rules, whenever an appropriate number of FCS frame has been correctly received.

5.2 - PERFORMANCE OF THE ACTUAL IMPLEMENTATION

In order to obtain performance results that match the actual HW design, a 4 Mbytes data blocks transmission has been simulated.
By referring to the two possible alternatives for the segmentation buffer implementation, it is important to estimate point out that using the SRAM the use of the Estimated Credit Procedure (procedure to estimate W, see [1]) (ECP) is not possible, and consequently only the ACK-N flow control mechanism, with N=W* , is allowed. The FCS source sends the whole data block and waits for the ACK-N frame arrival. The value of N (=W) is 1985 for 4 Mbytes data blocks transmission.

Table 5.1 - Results of 4Mbyte data blocks simulation (W=N=1985; d=0)

Observed statistic	FIFO buffer	SRAM buffer
ETEdelay (sec)	0.044	0.198
ACK-N return time (sec)	0.242	0.397
Throughput (Mbit/s)	131.8	80.4

Table 5.1 and fig. 5.2 show a comparison of the results obtained using a FIFO or SRAM segmentation buffer and maximum length frame transmission.
The talbe points out, for d=0 km, the worsening of the performances using a SRAM. It can be noted that the FIFO solution allows the target of 130Mbit/s to be reached; a simpler implementation solution utilizing SRAM leads to lower throughput performance.
Figure 5.2 shows for d=0 and d=45 km the IWU behaviour varying the window size W=N; a value of N equal to 32 frames (corresponding to 64 Kbytes data blocks) in sufficient to achieve an exploitation of the bandwidth close to maximum value, minimizing the problems related to cell loss in the ATM path; however, increasing W it is possible to make the throughput performance independet of the distance d.

* W = Is the maximum number of frames in transit
N = Number of frames that need to be received in order to the receiver send a ACK-N (W > N)

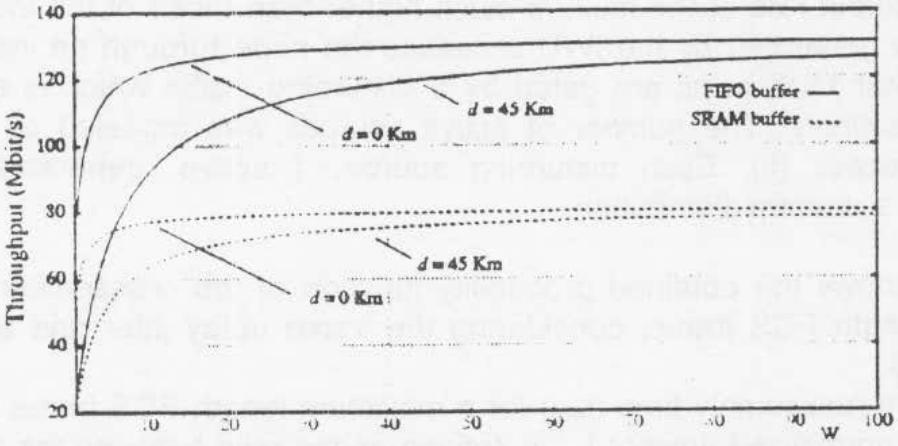

Figure 5.2 - Throughput vs window size for N=W, FIFO/SRAM buffers

Finally, the last parameter which has been studied is the reassembly timeout. This parameter indicates the maximum time interval allowed for the arrival of all the cells belonging to an FCS frame; i.e. the time elapsing between the SOF cell and the EOF cell arrivals. If this time expires, the reassembly process is aborted and all the arrived cells for the current frame in the receive buffer are discarded. The timeout value strictly depends on the cell delay jitter introduced by the ATM network.

For this purpose, an ATM switch has been modeled by means of a non-blocking, output queueing structure (fig. 5.3).

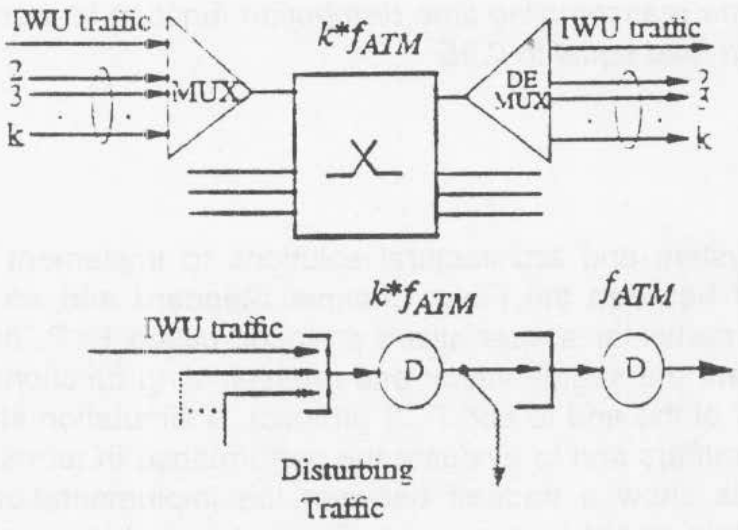

Figure 5.3 - ATM switch model

It consists of a cascade of a multiplexer, accessed by the incoming lines, a queue module followed by a demultiplexer output buffering functions. The internal bit rate of the switch (output rate of the mux) is much higher than those of the incoming lines. The cell flow generated by the IWU accesses the node through an individual MUX port. The other MUX ports are gated by a disturbing traffic which is originated by other ATM sources. The number of active sources was modeled by means of a Bernoulli process [5]. Each disturbing source, if active, generates ATM cells according to a uniform distribution.

Figure 5.4 shows the obtained probability function of the reassembling time for a maximum length FCS frame, considering the frame delay jitter and a switch load equal to 0.95.
The minimum reassembly time (t_{min}) for a maximum length FCS frame is a equal to 122 ms; the normalized timeout t_{out} is defined as the ratio between the reassembling time and t_{min}.
As it can be noted, a timeout value equal to 1.5 is sufficient to avoid frame loss in the reassembly process, when only one ATM switch is present.

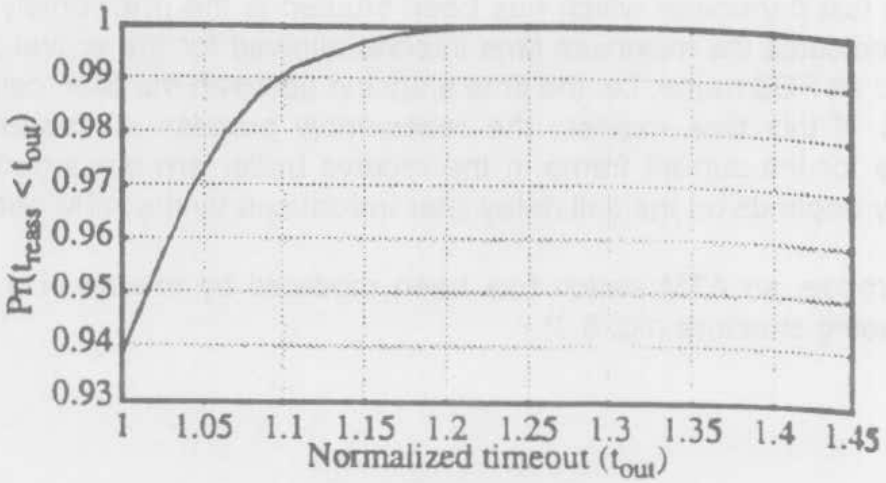

Figure 5.4 - Frame reassembling time distribution function vs normalized timeout for switch load equal to 0.95.

6. Conclusion

In this paper, system and architectural solutions to implement a high throughput interworking unit between the Fiber Channel Standard and an ATM network has been shown. In particular a specialized protocol, called FAP, has been defined in order to implement the segmentation and reassembling functions and to guarantee the transparency of the end to end FCS protocol. A simulation study was performed to size the IWU buffers and to evaluate the performance in terms of throughput. The simulation results show a tradeoff between the implementation complexity when large blocks of data must be segmented. The first proto-type has been implemented with the SRAM solution, but the final goal is to implement the FIFO strategy. Currently, the adaptations of the FAP to the last version of the AAL5 protocol is being studied.

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